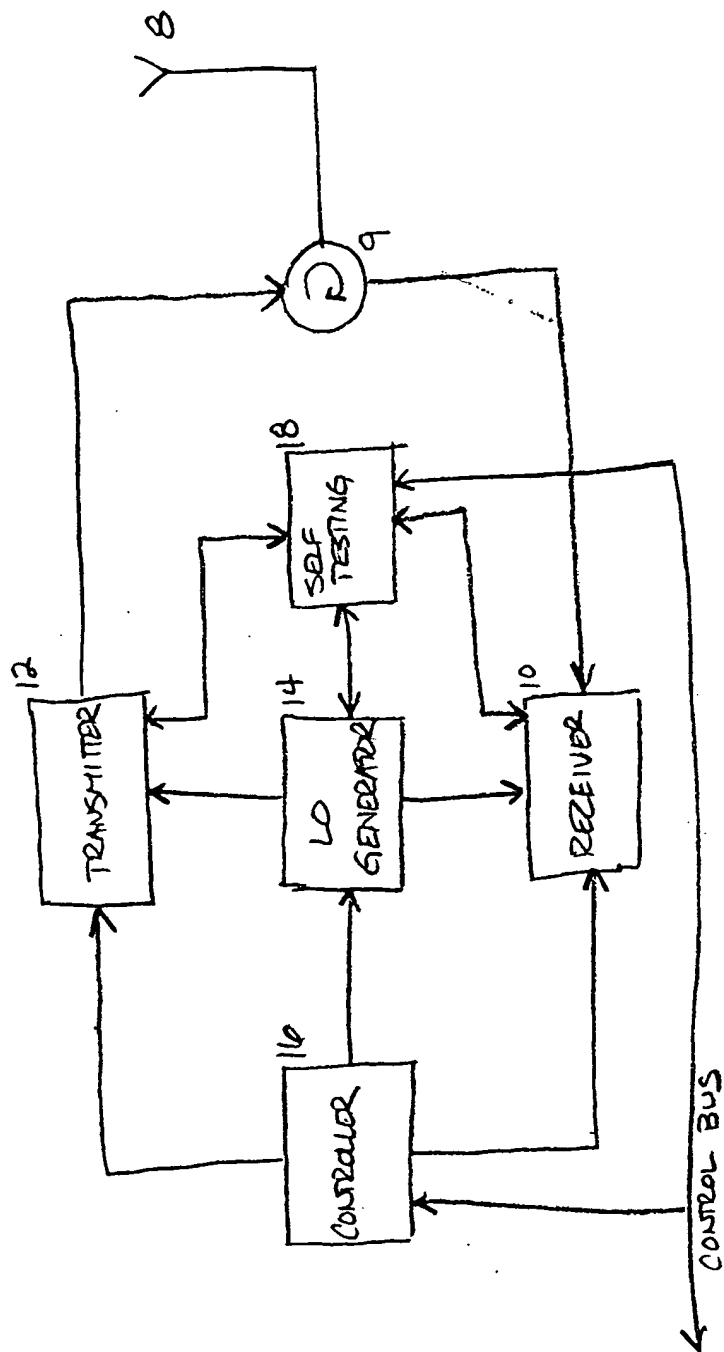


[illegible]

151

2000

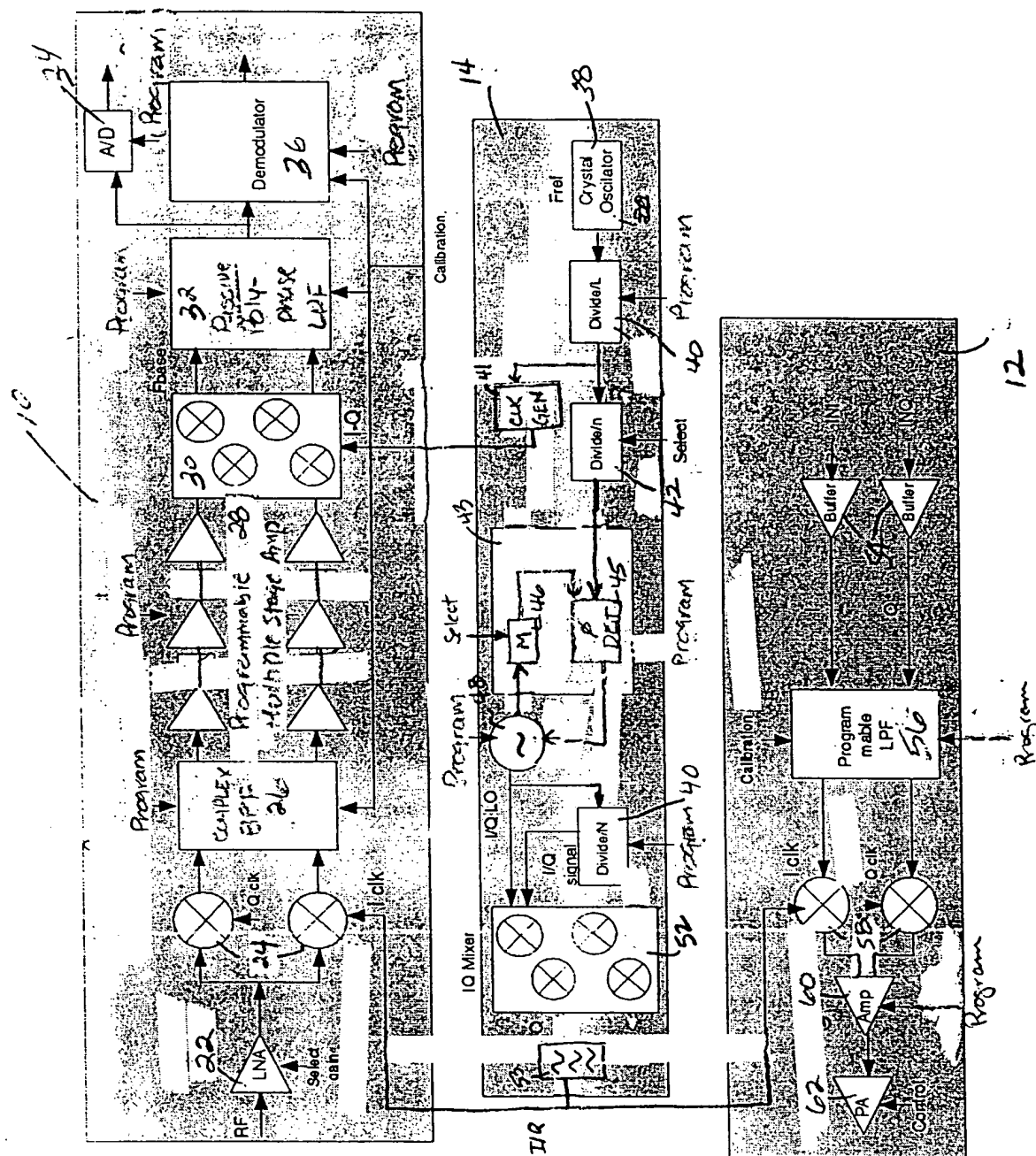
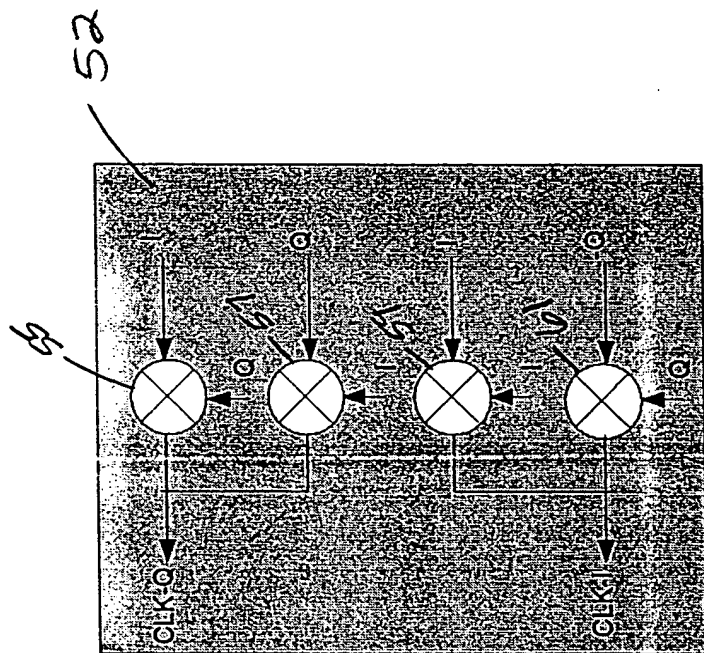


Fig. 2



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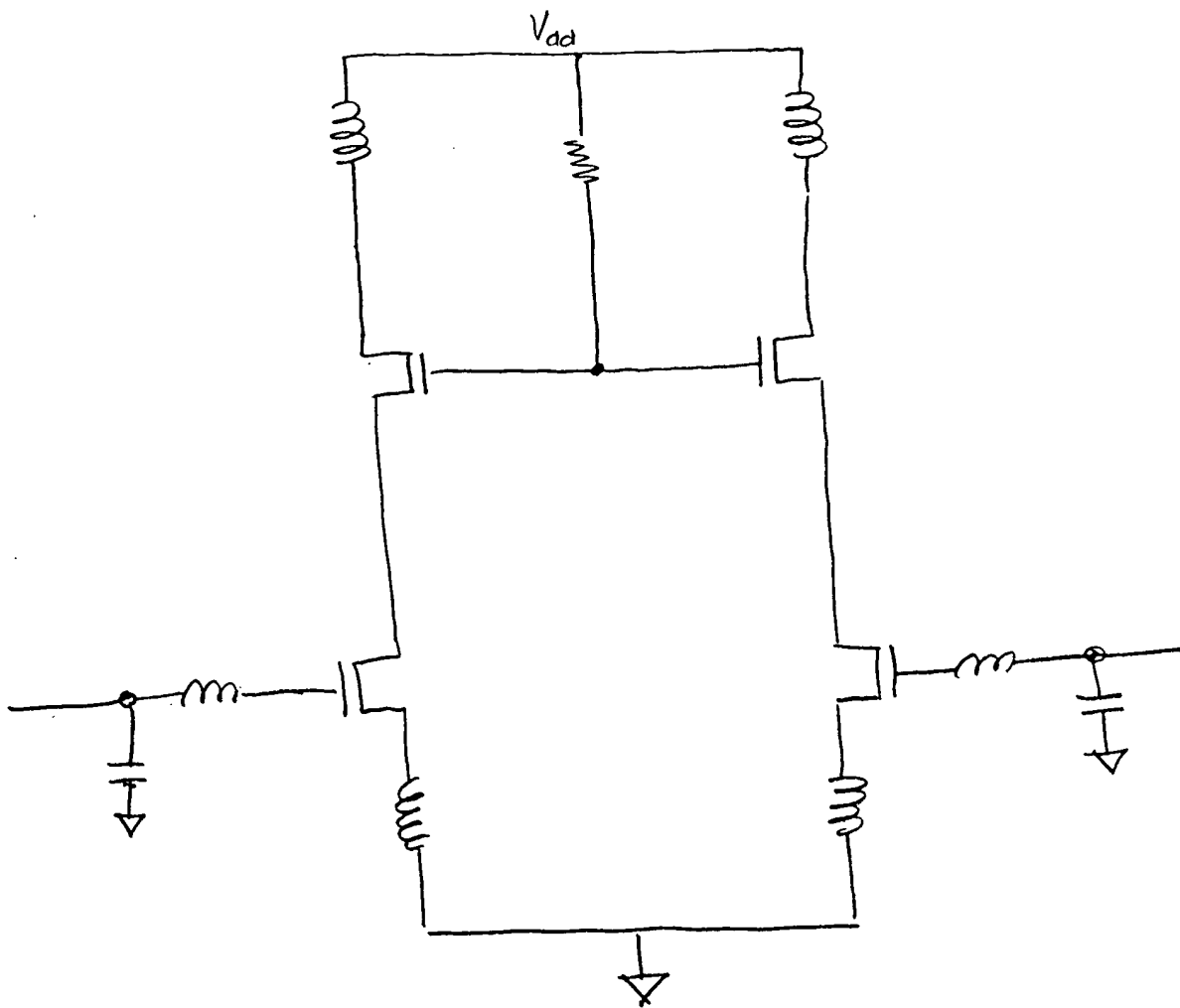


FIG. 4(a)

FIG. 4

\_\_\_\_\_



FIG. 5

000001-22916960

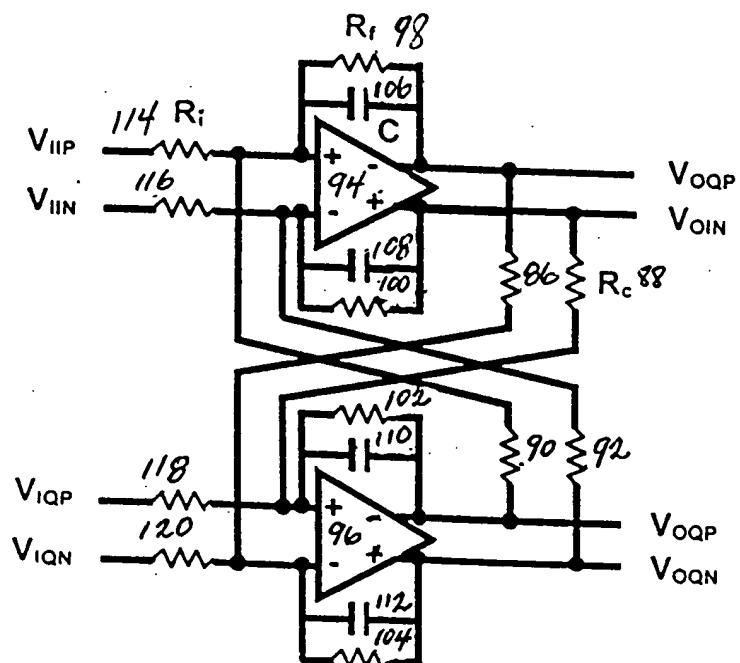


FIG. 6

**FIG. 7**



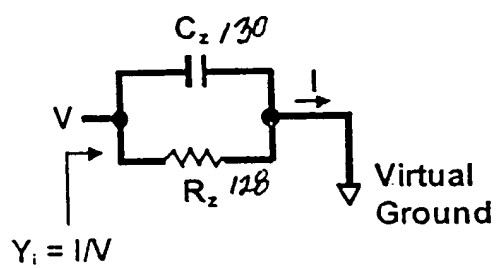


FIG. 8

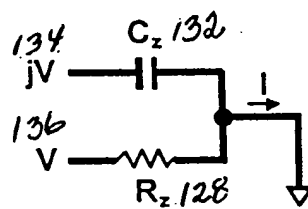


FIG. 9

000007 26516960

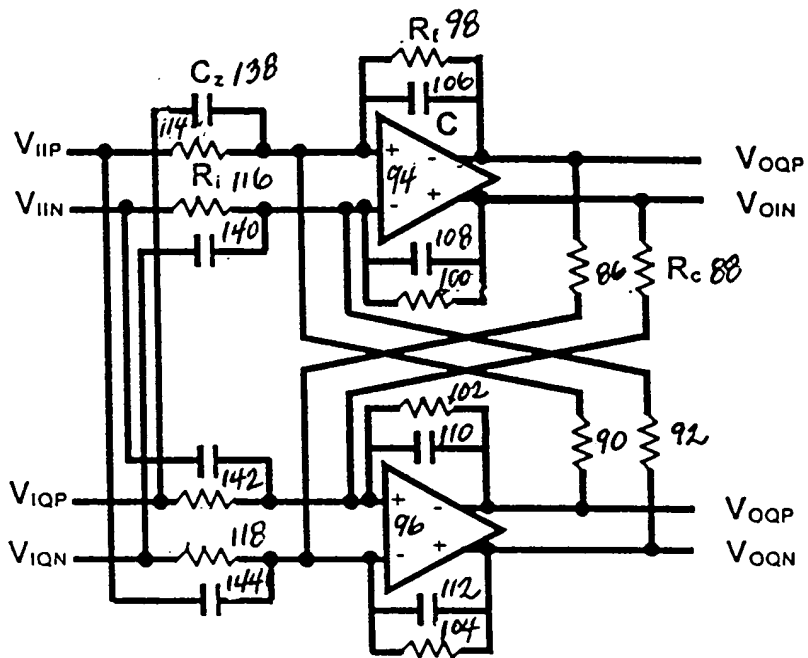
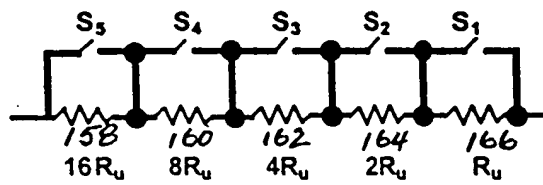
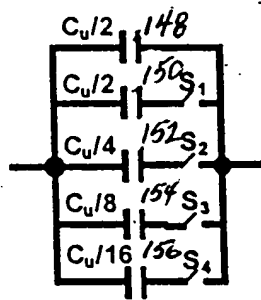


FIG. 10

Figure 1 is a plot of Attenuation (dB) versus Frequency (MHz) for the 146 MHz band. The x-axis represents Frequency in MHz, ranging from -6 to 6. The y-axis represents Attenuation in dB, ranging from -60 to 10. The plot shows a sharp dip in attenuation at approximately 2 MHz, labeled "Zeros at:  $2 \pm 1.3$  MHz". The attenuation is approximately -15 dB at 0 MHz and -15 dB at 6 MHz, with a peak of approximately -10 dB at 2 MHz.

FIG. 11



00501532-101800

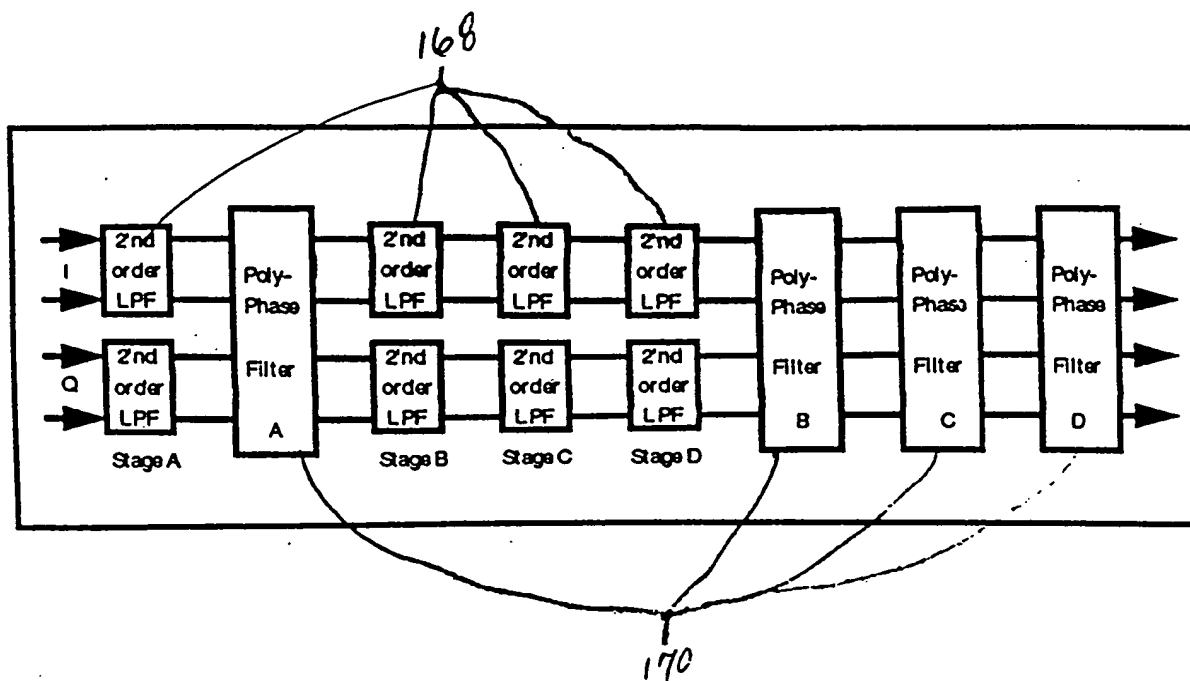


FIG. 13

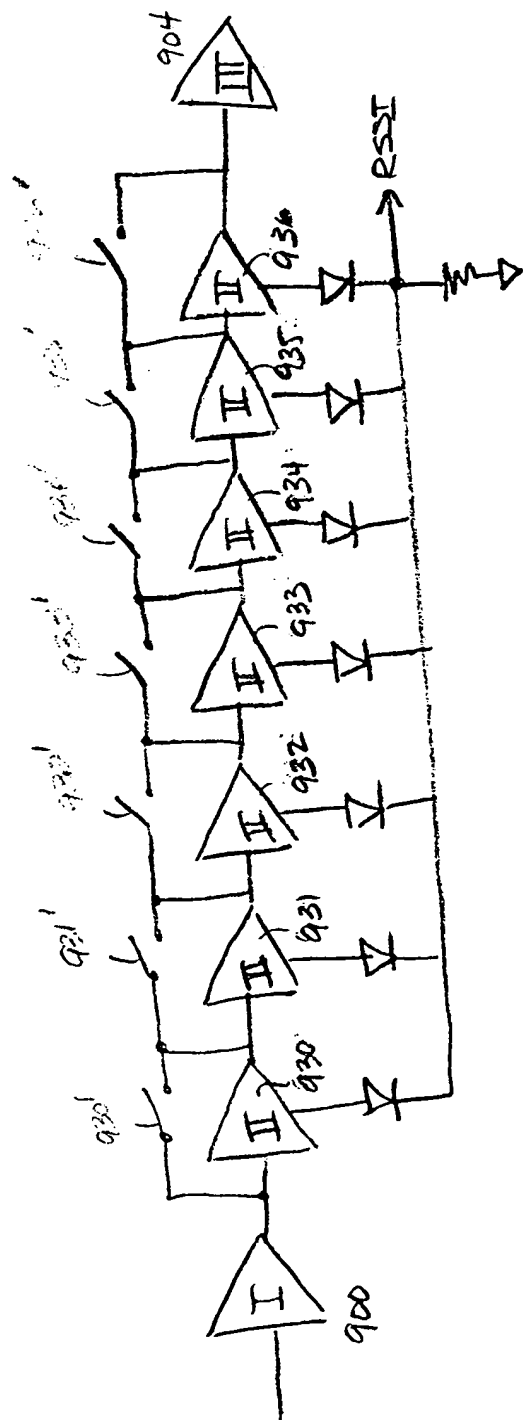


FIG. 14

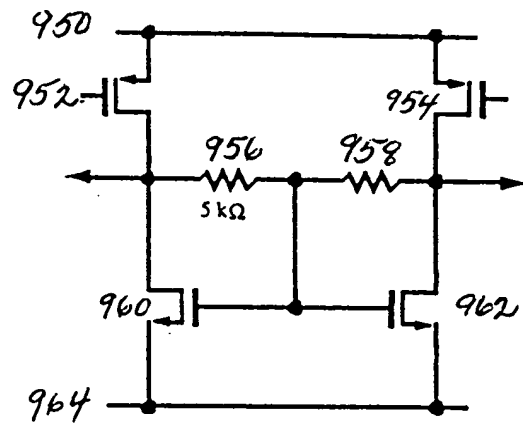
[illegible]

FIG. 15

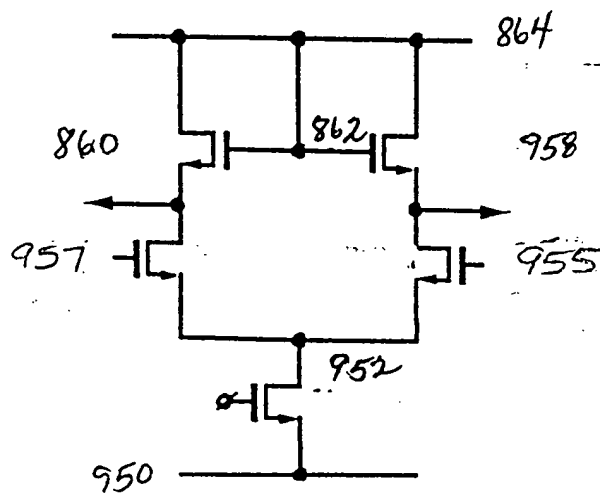


FIG. 16(a)



✓

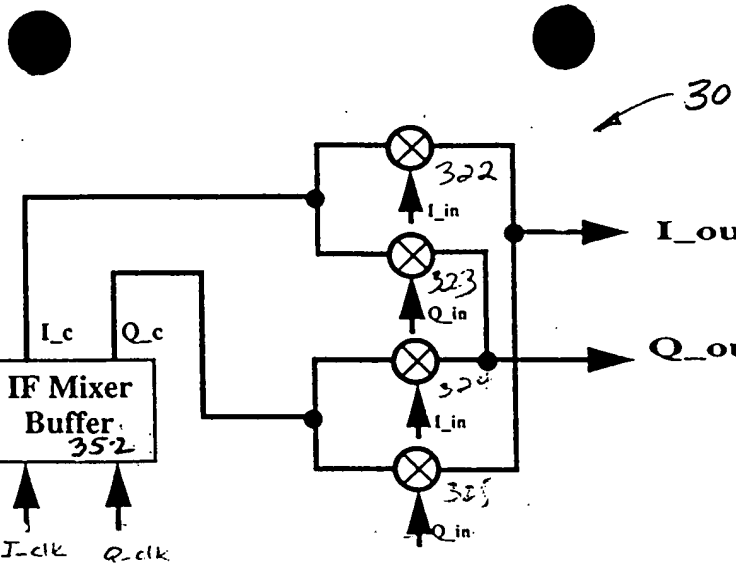


FIG. 17(a)

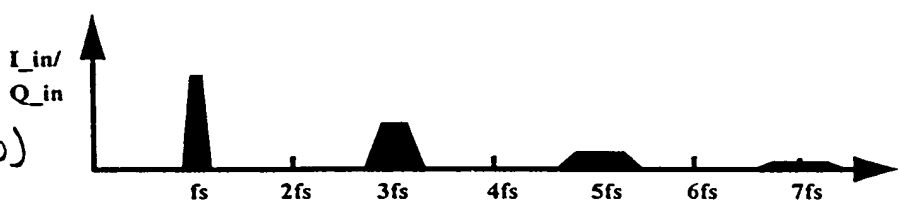


FIG. 17(b)

Limited IF Signal Spectrum

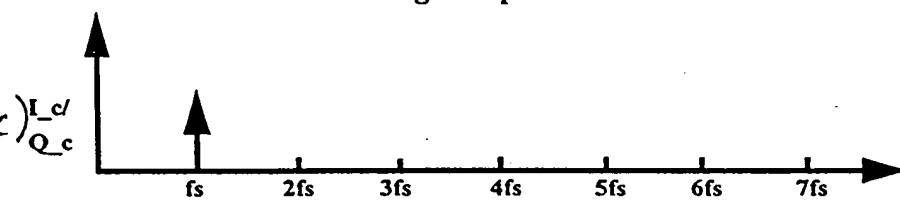


FIG. 17(c)

Sinusoidal Input Spectrum

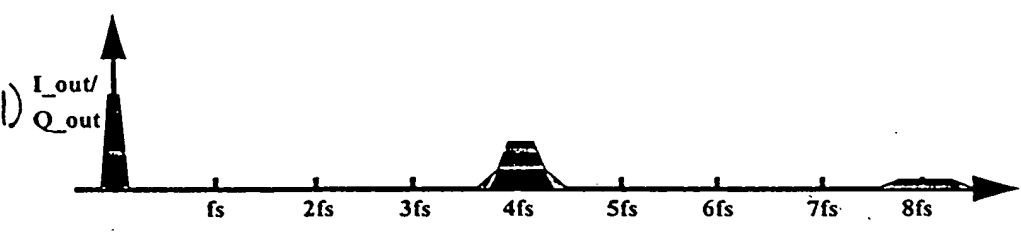


FIG. 17(d)

IF Mixer Output Spectrum

00601632-101800

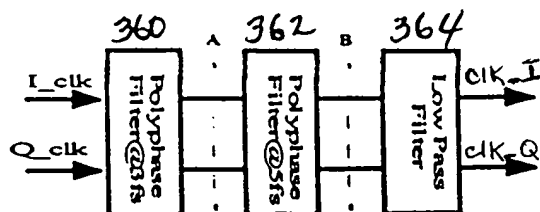


FIG. 18

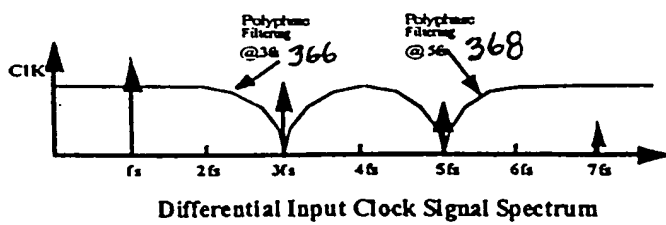


FIG. 19(a)

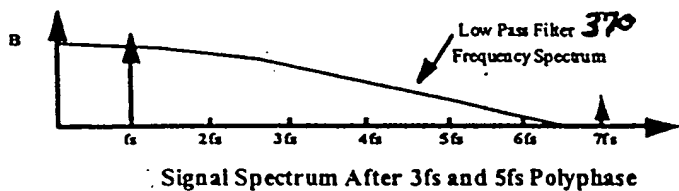


FIG. 19(b)

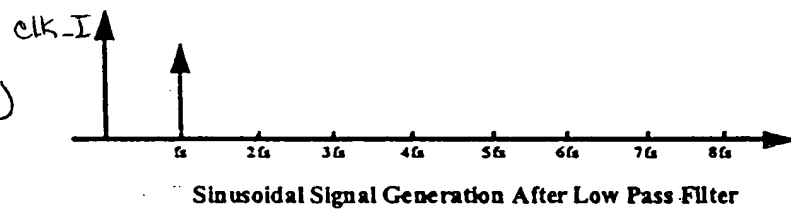
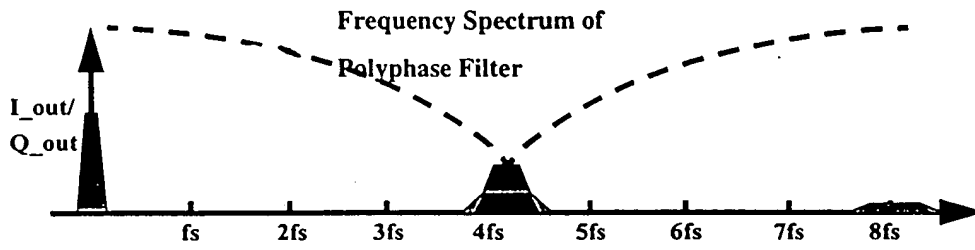


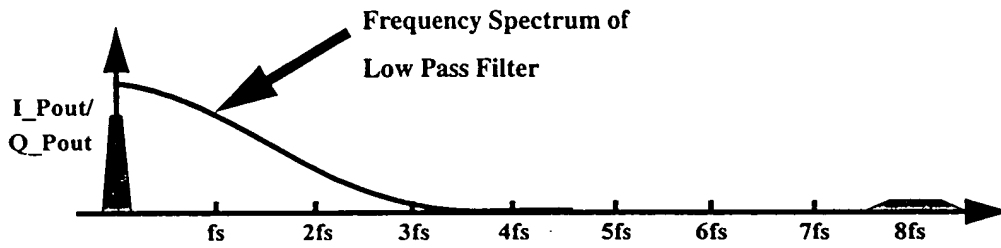
FIG. 19(c)

00504432-101800



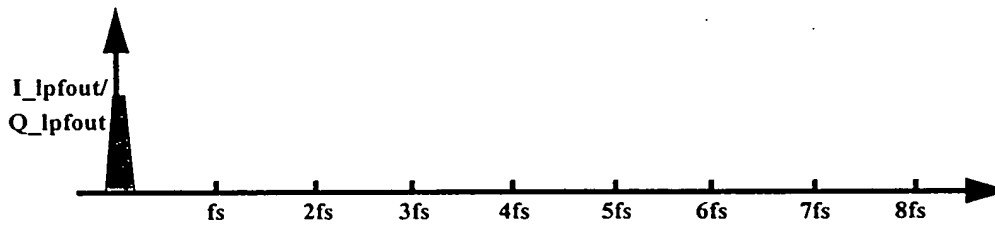
Signal Spectrum at Polyphase Input

FIG. 20(a)



Signal Spectrum at Polyphase Output

FIG. 20(b)



Signal Spectrum at Low Pass Filter Output

FIG. 20(c)

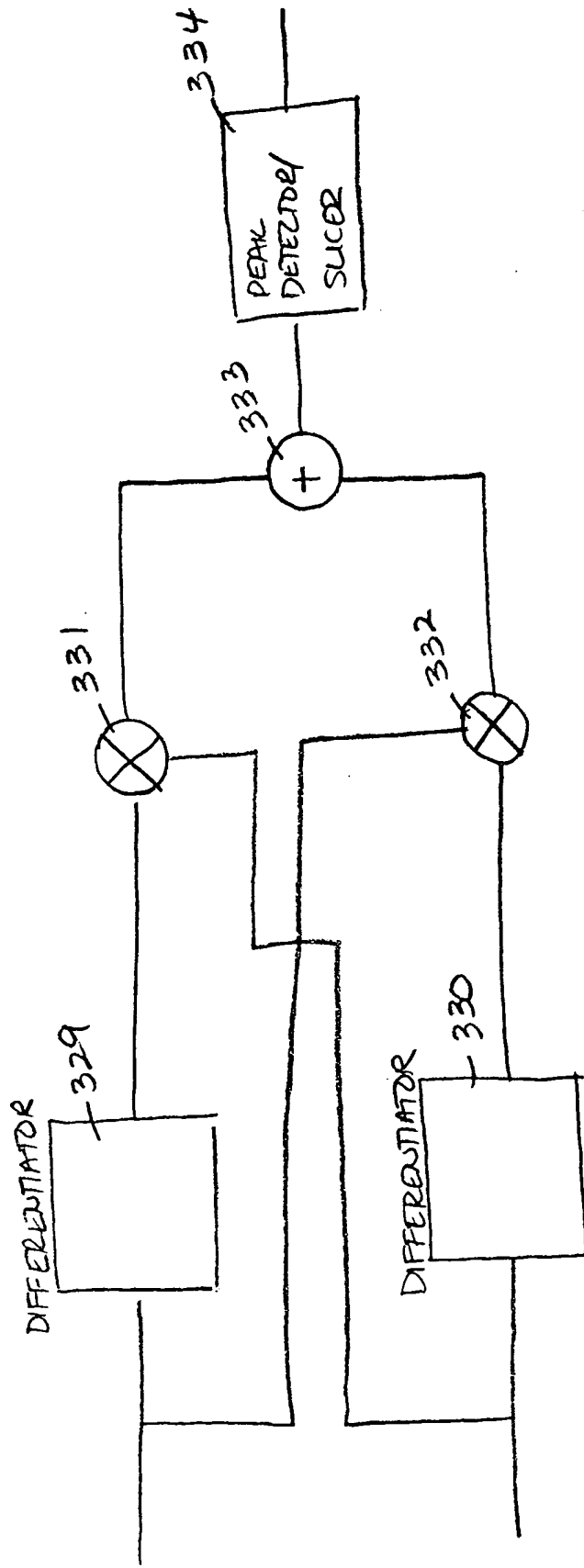


FIG. 21

# 2025年12月12日

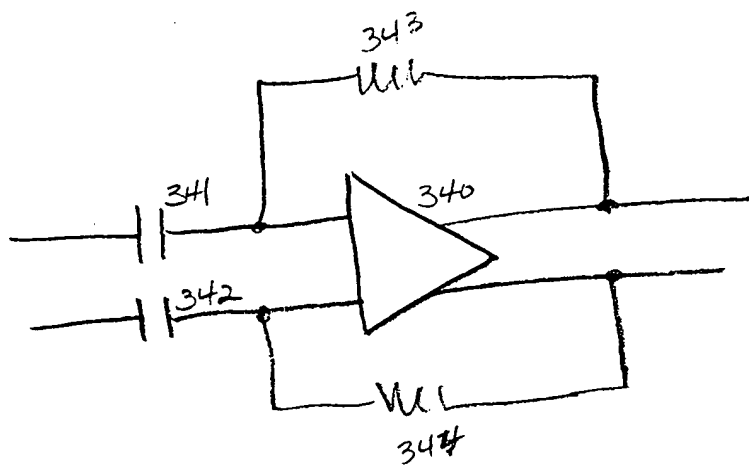


FIGURE 22

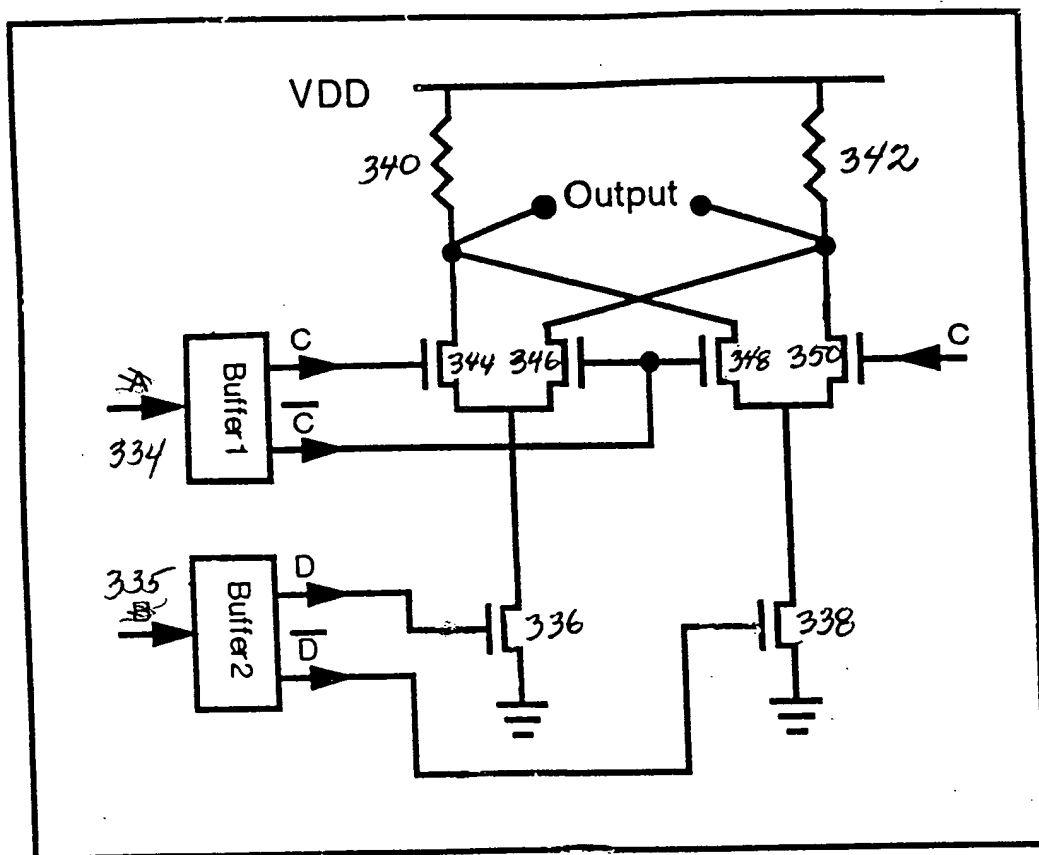


FIG. 23

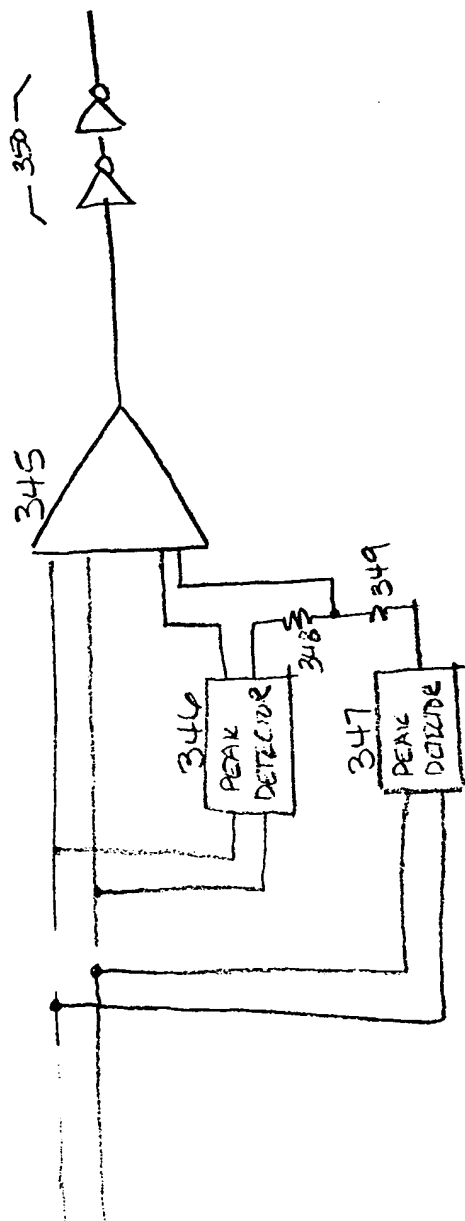


FIGURE 24



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FIG. 25

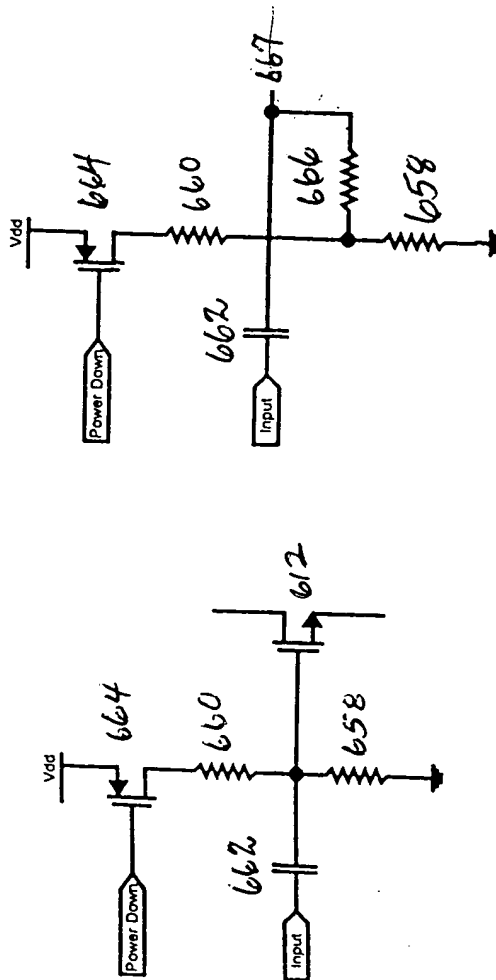


FIG. 26(a)

FIG. 26(b)

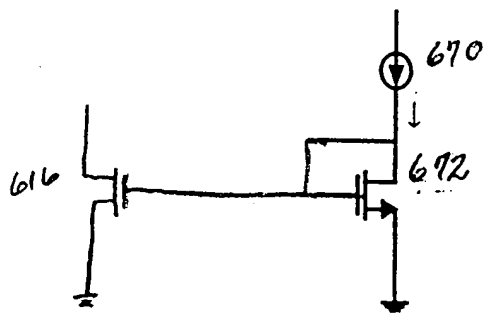


FIG. 27

FIG. 28

000001 22316500

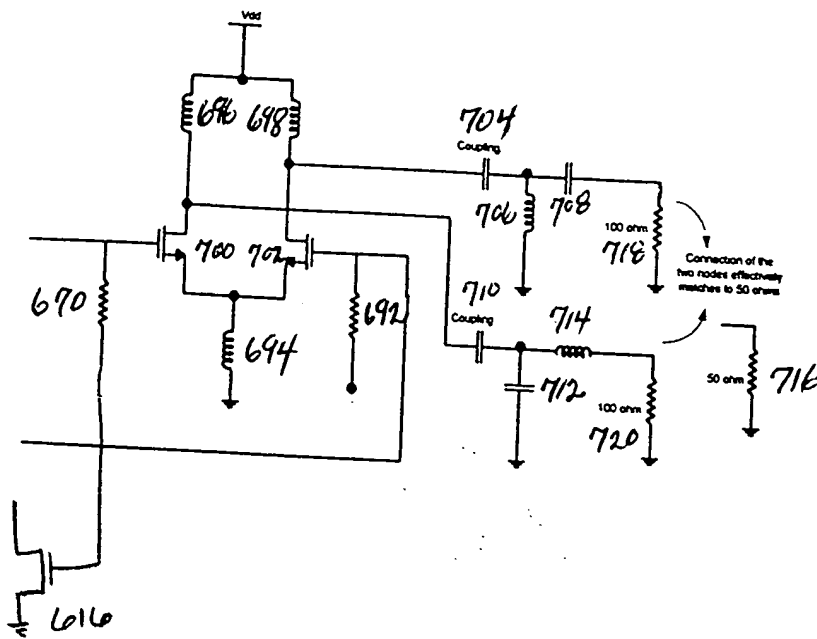


FIG. 29

FIG. 30

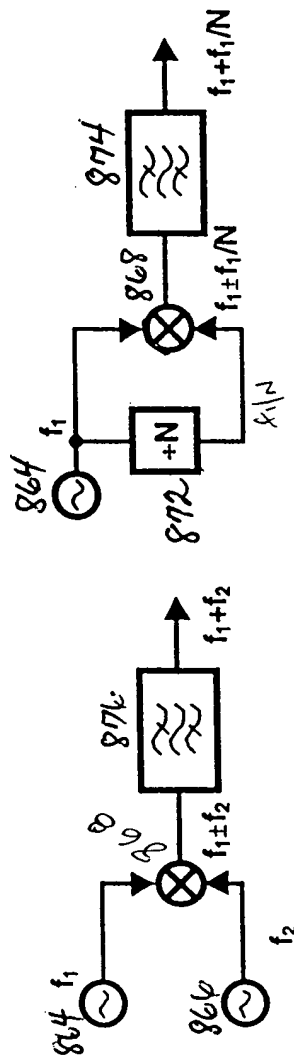


FIG. 31 (a)

FIG. 31 (b)

FIG. 32



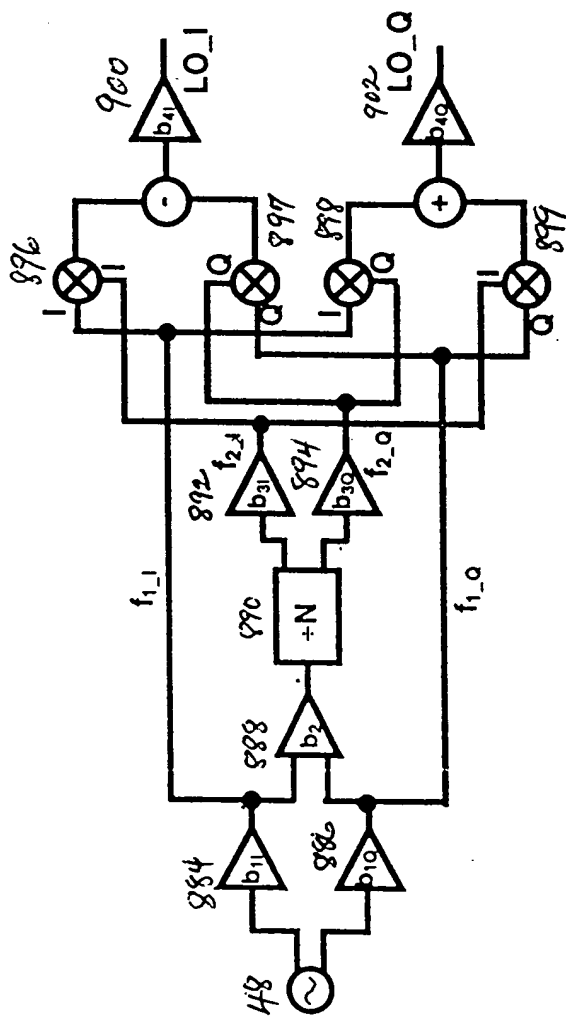


FIG. 33

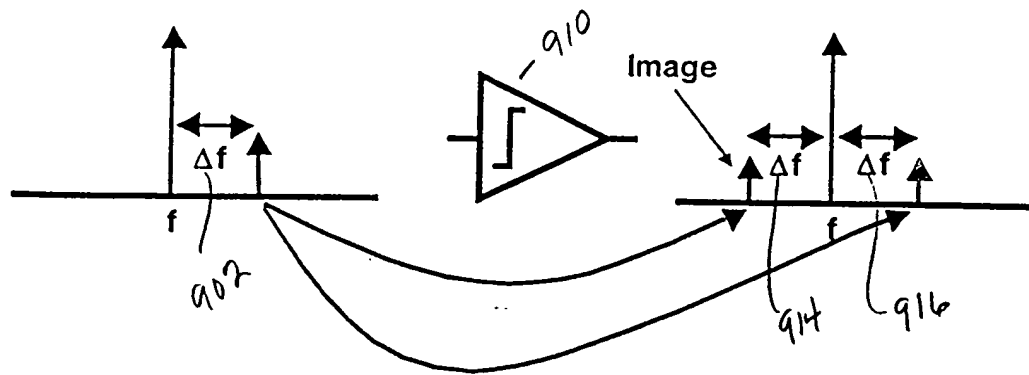
[illegible]

FIG. 33(a)

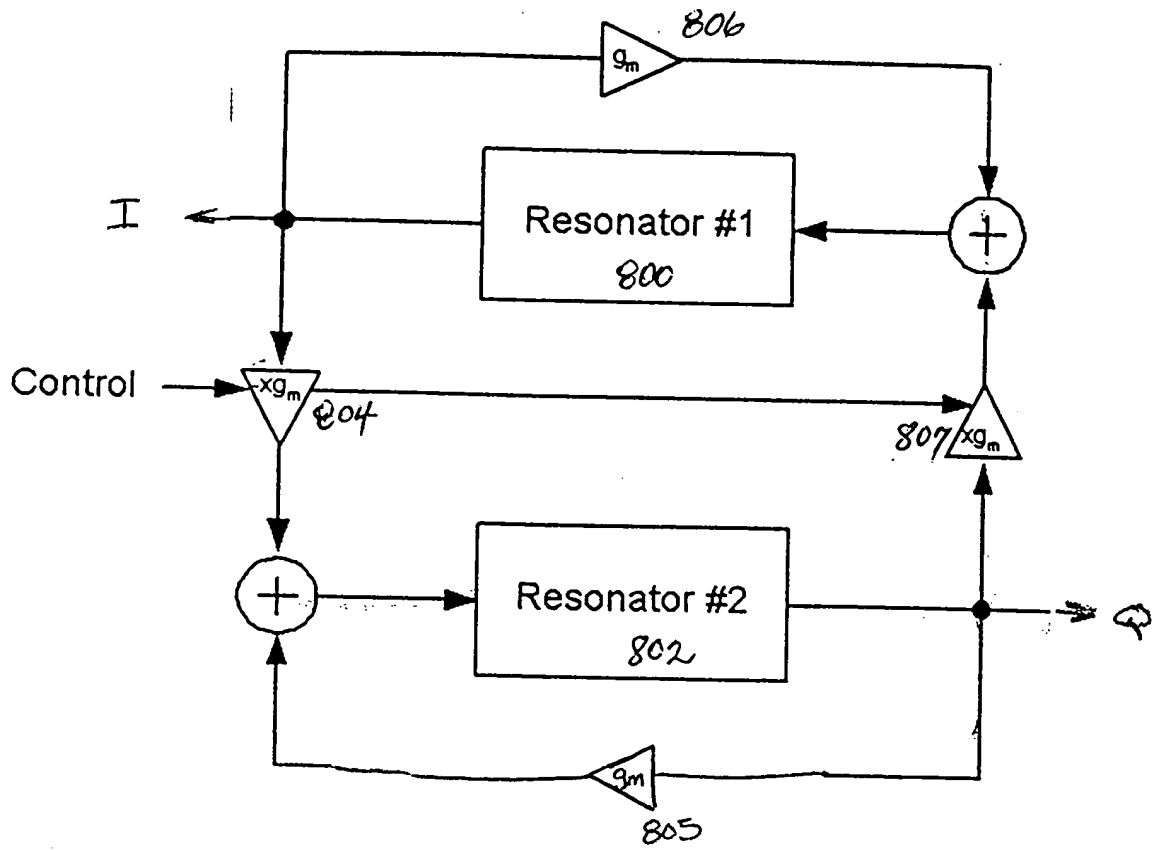


FIG. 34

008707-22976960

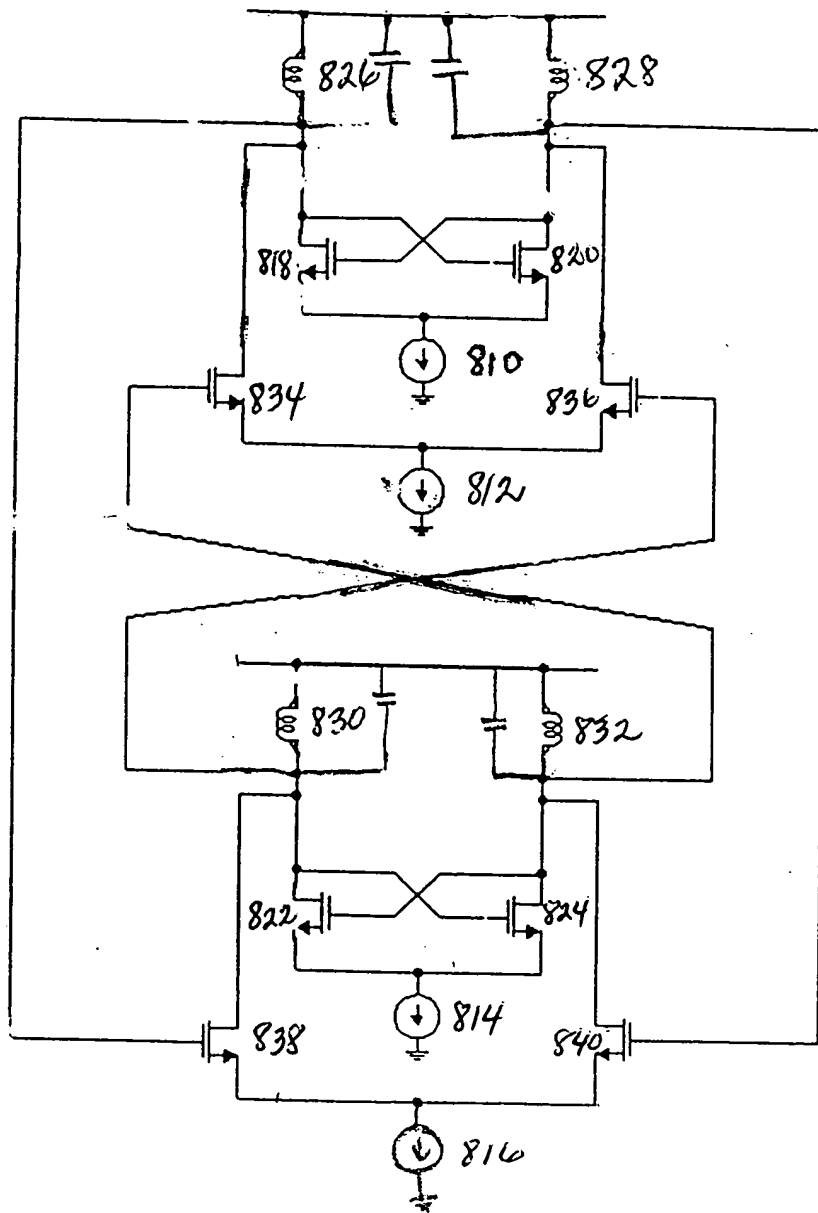


FIG. 35

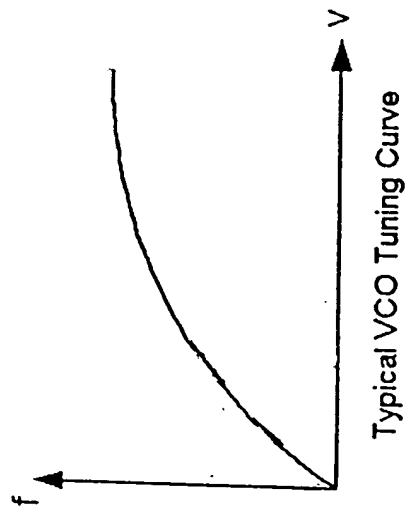


FIG. 36(a)

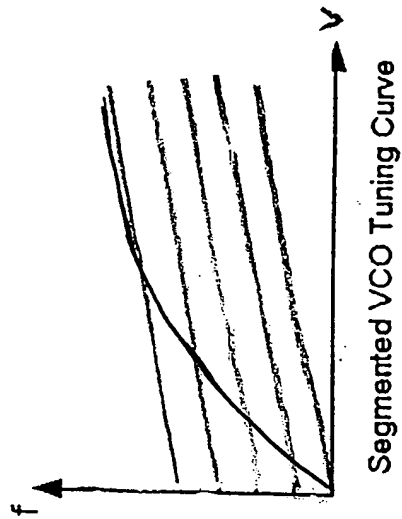


FIG. 36(b)



FROM  
EXTERNAL  
PROCESSING  
DEVICE

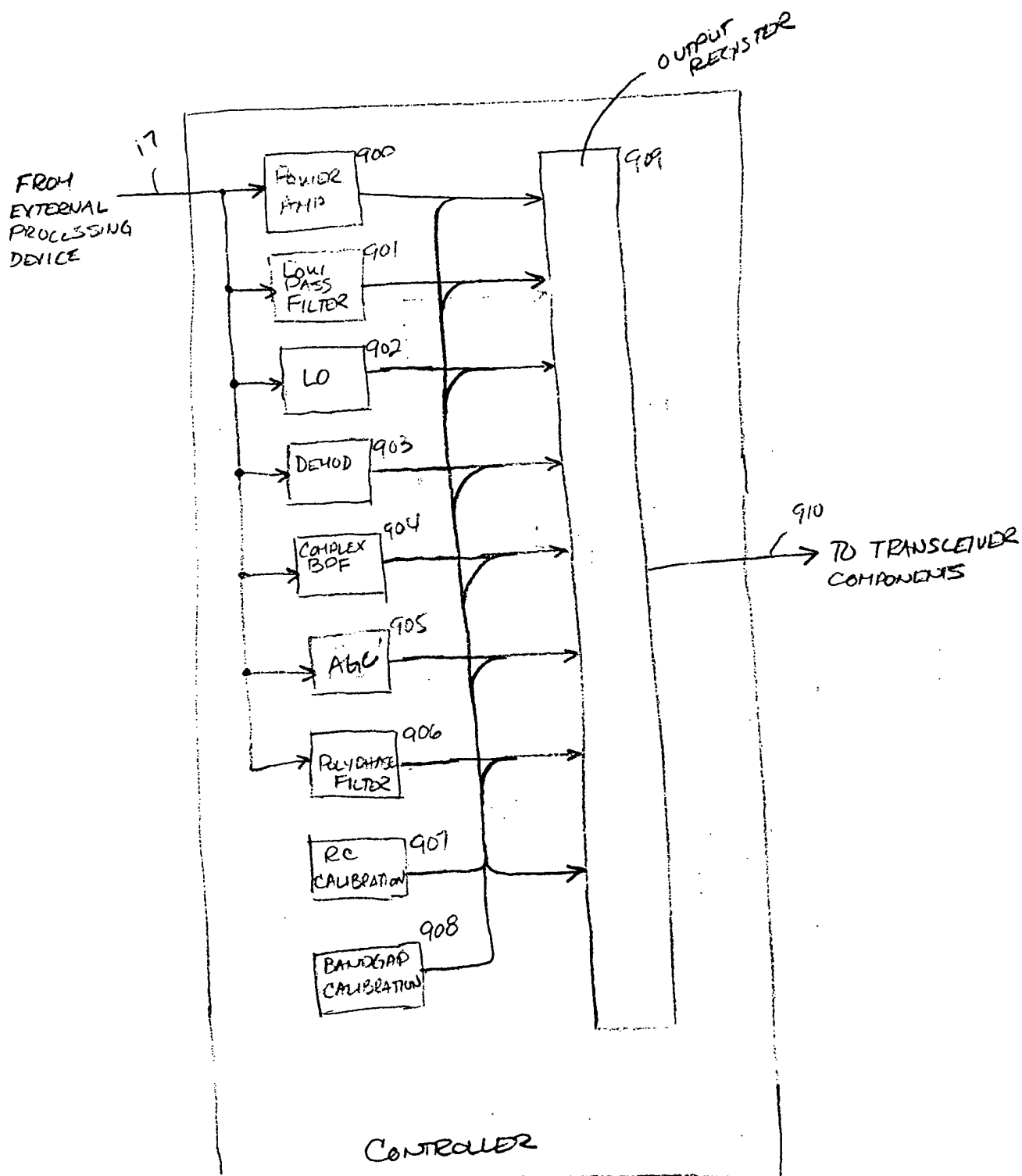


FIGURE 38

00591632-101300

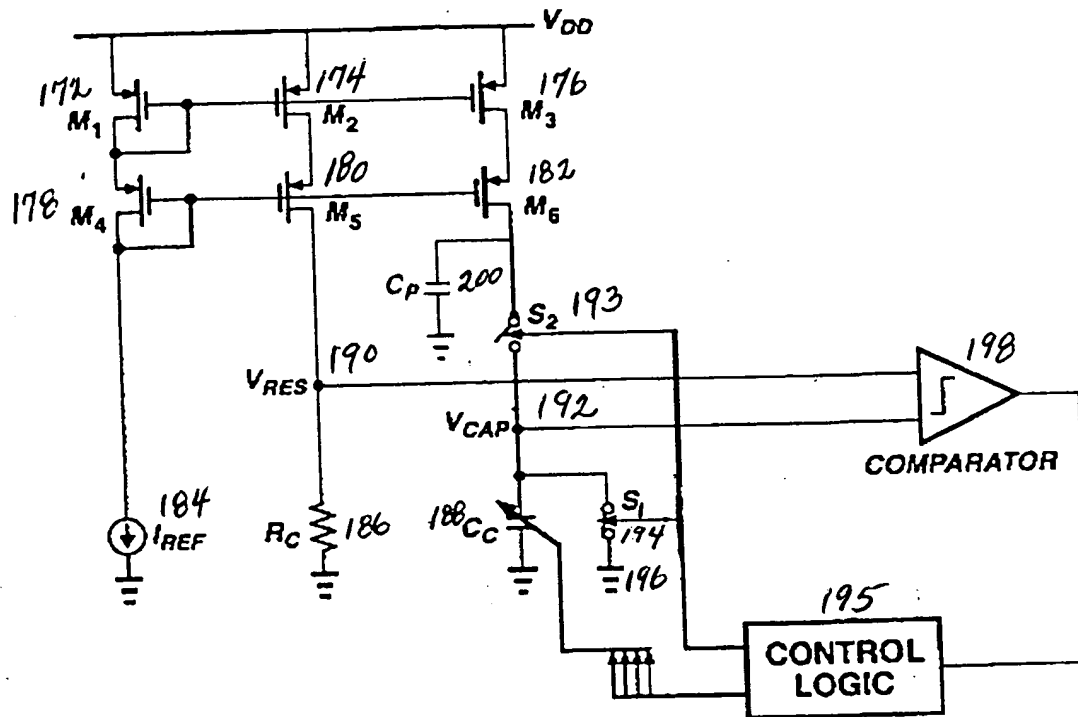


FIG. 39



FIG. 1 is a block diagram of a PLL circuit. The circuit includes a divider (280) that receives an input signal  $I$  and  $Q$  and outputs  $X_{IN}$ .  $X_{IN}$  is fed into two polyphase filters, POLYPHASE A (282) and POLYPHASE B (282). POLYPHASE A outputs  $X_A$  and  $\langle C_A \rangle$ . POLYPHASE B outputs  $X_B$  and  $\langle C_B \rangle$ .  $X_A$  and  $X_B$  are fed into two RSSI (Radio Frequency Signal Interference) blocks (284). The outputs of the RSSI blocks are fed into a phase detector (286) and a control logic block (286). The control logic block (286) receives a clock signal  $CK$  (250 kHz) and outputs a control signal to the divider (280). The phase detector (286) also outputs a control signal to the divider (280). The control signal is fed back to the divider (280) to complete the feedback loop.

FIG. 40

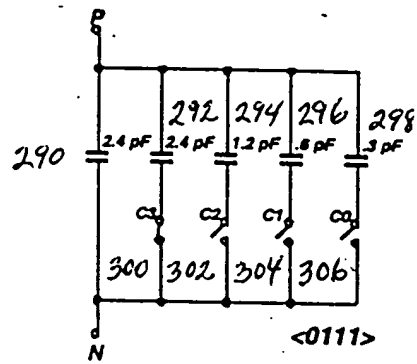


FIG. 41

00001531-10100  
00001531-10100

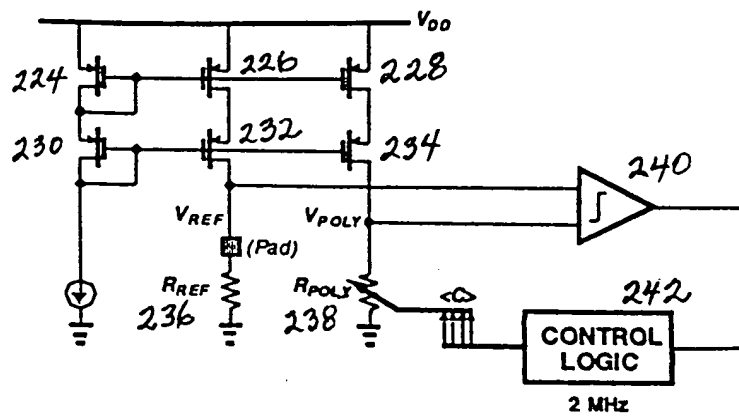


FIG. 42

FIG. 43

FIG. 44

FIG. 45

000007-26376960

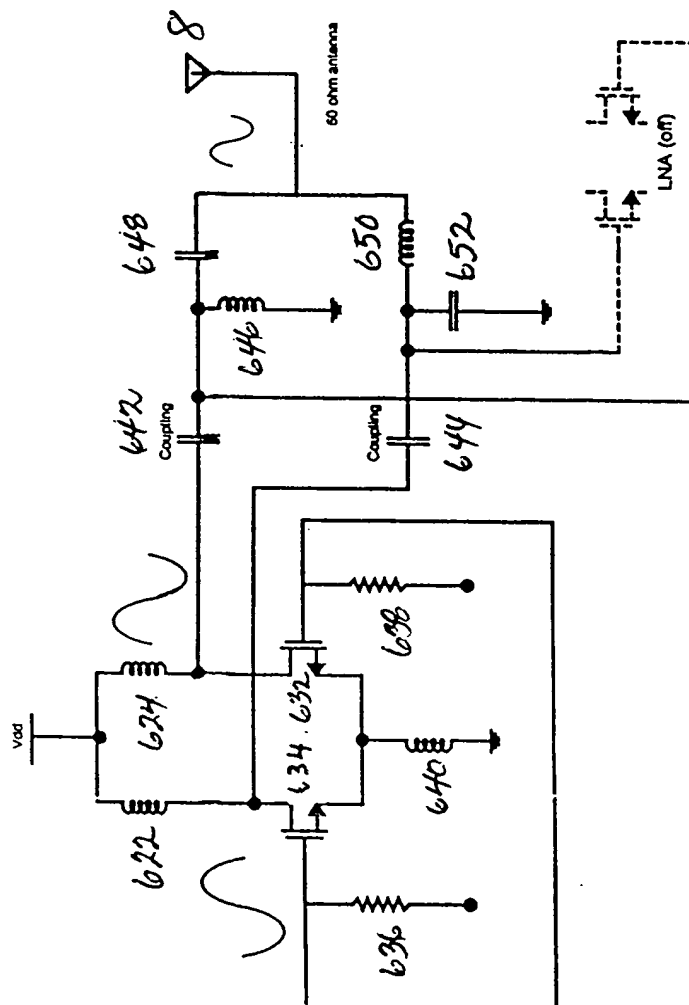


FIG. 46

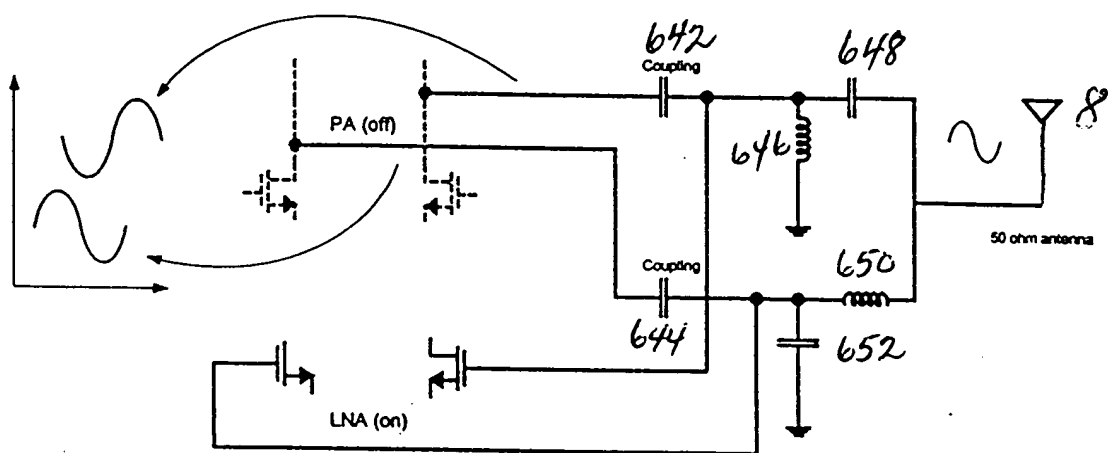


FIG. 47